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DIGITAL CLOCK DESIGN BASED ON PROTEUS SIMULATION SOFTWARE

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Abstract: In the context of the limitations of traditional timekeeping tools, the continuous progress of electronic and digital technologies, the increasingly diversified needs of different application scenarios, and the ever-increasing requirements of user experience, the research on digital clock circuit design has emerged and continues to develop. This digital clock circuit employs a cascaded configuration of 74160 adder counters to achieve sexagesimal counting for seconds and minutes, and twenty-four-ary counting for hours, thereby enabling the counting of hours, minutes, and seconds, which are displayed via seven-segment displays. Simulation verification was conducted using Proteus simulation software. The circuit operates stably within the timing range of 00:00:00 to 23:59:59. The second counter switches to the minute counter every 60 seconds, the minute counter switches to the hour counter every 60 minutes, and the hour counter automatically resets every 24 hours. This paper provides low-cost and easy to reproduce the simulation circuit, on the understanding and mastery of the principle of digital clock has a certain role in assisting, for the subsequent design of complex digital systems to lay the foundation.
Keywords: Proteus; Digital clock; Imulation

1 INTRODUCTION

Proteus simulation software developed by the UK Labcenter Electronics, is an integrated electronic design automation (EDA) tool, known for its comprehensive functionality and ease of operation, widely used in electronic circuit design, teaching and engineering development [1]. The software contains core modules such as circuit schematic drawing, virtual simulation, PCB design, etc., which can realize the whole process from design to plate making: the circuit design module supports multi-layer drawing and intelligent operation; the simulation module is based on the SPICE kernel, which can complete the dynamic simulation of all kinds of circuits and multi-mode analysis; the PCB module provides automatic routing and rule checking, and can generate production documents that meet the standards. Its rich component library covers basic components, microcontrollers, sensors and virtual instruments, which can meet the diversified needs from basic circuit design to complex system simulation, providing effective guidance for circuit design and development.

The timing results of digital clocks are very different from those of mechanical clocks, which visually present the hours, minutes, seconds, and even the year, month, and day in a clear digital form. This kind of display makes it unnecessary for people to speculate the time through the position of the hands like looking at a mechanical clock, and it can be read quickly and accurately, which is very intuitive and provides great convenience for various industries [2-3]. This paper uses Proteus simulation software to design a digital clock circuit. The circuit employs cascaded 74160 adder counters to implement sexagesimal counting for seconds and minutes, and twenty-four-ary counting for hours. This enables the counting of hours, minutes, and seconds, with the corresponding time displayed via seven-segment displays. Optimize the circuit logic with the help of simulation verification, and finally realize the counting and clear display of hours, minutes and seconds to meet the basic needs of daily time observation.

2 DIGITAL CLOCK CIRCUIT DESIGN

The digital clock circuit design is shown in Figure 1. The second module begins counting under the influence of a clock pulse signal [4] with a period of 1 second. When the second module completes counting 60 seconds, it sends a “second feed” signal to the minute module. The minute module begins counting under the “second feed” signal. When the minute module completes counting 60 minutes, it sends a “minute feed” signal to the hour module. The hour module begins counting under the “minute feed” signal. The time of the digital clock is displayed by the digital tube of the hour module, minute module and second module respectively, realizing the counting from 00:00:00 to 23:59:59 [5-6].

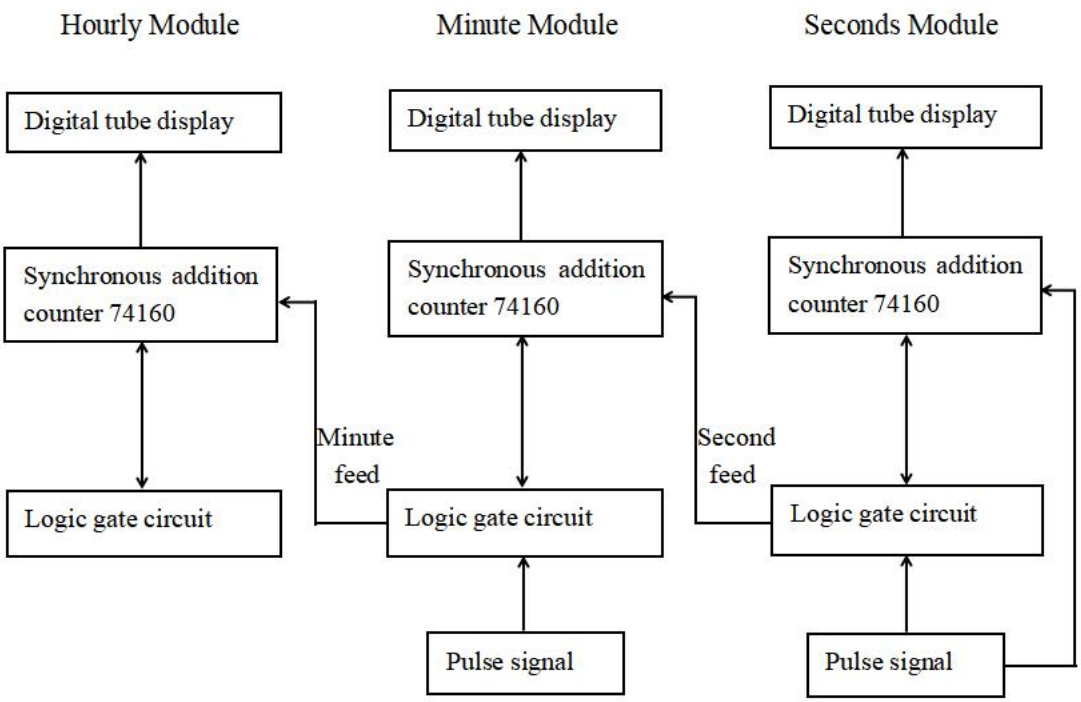

Figure 1 Digital Clock Circuit Design

2.1 Digital Tube Display

Digital tube displays are used to show the numbers corresponding to "hours", "minutes" and "seconds" [7]. In a variety of displays, seven-segment digital tube is more widely used, seven-segment digital tube is divided into two categories of common anode and common cathode. In this paper, the seven-segment digital tube with common anode is used to display Arabic numerals. Common anode digital tube of the seven light-emitting tube anode connected together to a high level, the cathode connected to a low level of the light-emitting tube is lit. Each segment is labeled as a, b, c, d, e, f, g. By controlling the high and low levels of these segments, the corresponding numbers can be displayed.

2.2 Counter Design

The design of the counter is a key part of the digital clock. In this paper, a synchronous addition counter 74160 is used for counting [8], 74160 is a binary synchronous modulo 10 addition counter, which has four independent counting outputs, each output corresponds to one binary bit, and its function is shown in Table 1.

Table 1 Synchronous Addition Counter 74160 Function Table

					Preset Data Input				Exports				
$\overline{CLR}$	$\overline{LOAD}$	ENP	ENT	CLK	D_3	D_2	D_1	D_0	Q_3	Q_2	Q_1	Q_0	Operating mode
0	×	×	×	×	×	×	×	×	0	0	0	0	Asynchronous Reset
1	0	×	×	↑	d_3	d_2	d_1	d_0	d_3	d_2	d_1	d_0	Synchronous Counting
1	1	0	×	×	×	×	×	×	Remain				Data Retention
1	1	×	0	×	×	×	×	×	Remain				Data Retention
1	1	1	1	↑	×	×	×	×	Decimal number				Additive Counting

2.2.1 Seconds module design

In the seconds module set up two 74160 counters, respectively, the “seconds” of the units digit and tens digit, “seconds” of the units digit using decimal counting system, “seconds” of the tens digit using senary counting system. “Seconds” in the units digit counter, when $\overline{CLR}$ = $\overline{LOAD}$ = ENP = ENT = 1, and in the input clock pulse CLK rising edge of the role of the units digit counter for 0000-1001 addition count. When the units digit counter is 1001 and its output signal RCO is high, then $\overline{CLR}$ = $\overline{LOAD}$ = ENP = ENT = 1 in the tens digit counter, and under the action of the rising edge of the input clock pulse CLK, the tens digit counter carries out the addition count of 0000-0101. When the tens digit counter of the seconds module is 0101 and the units digit counter is 1001, the logic gate circuit is used to make the tens digit counter pin $\overline{LOAD}$ low, at which time the tens digit counter $\overline{LOAD}$ = 0, $\overline{CLR}$ = ENP = ENT = 1, and the tens digit counter of the seconds realizes synchronous counting under the action of the rising edge of the

input clock pulse CLK. With the tens digit counter of the seconds module at 0101 and the units digit counter at 1001, the seconds module feeds one bit to the minutes module through the logic gate circuit [9-10]. The circuit design of the seconds module and the minutes module is shown in Figure 2.

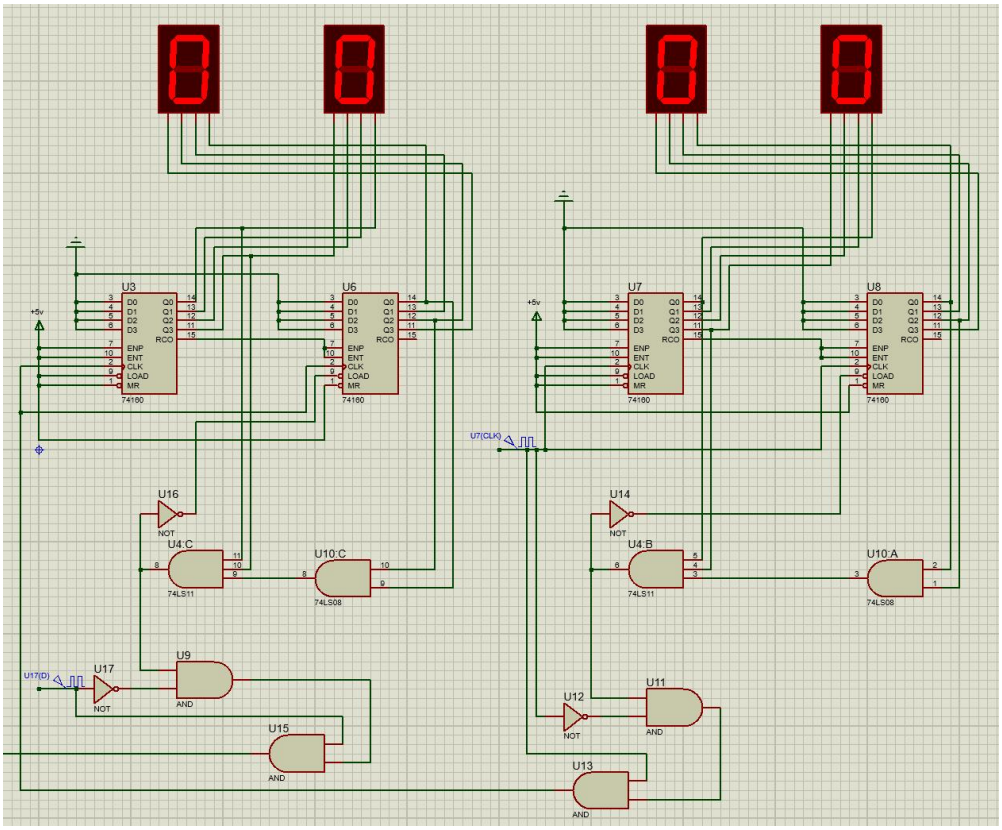

Figure 2 Seconds and Minute Modules for Digital Clocks

2.2.2 Minute module design

Similarly, two 74160 counters are set up in the minute module to represent the units digit and tens digit of "minutes". The units digit of "minute" is in decimal counting system, and the tens digit of "minute" is in senary counting system. When the minute module receives the rounding signal from the seconds module, in the minute module, its units digit counter $\overline{CLR}$ = $\overline{LOAD}$ = ENP = ENT = CLK= 1, and the units digit counter carries out the addition counting from 0000 to 1001. When the units digit counter is 1001 its output signal RCO is high, at this time the tens digit counter $\overline{CLR}$ = $\overline{LOAD}$ = ENP = ENT = CLK= 1, the tens digit counter carries out the addition count of 0000-0101. When the tens digit counter of the minute module is 0101 and the units digit counter is 1001, the logic gate circuit is used to make the pin $\overline{LOAD}$ of the tens digit counter low, at this time, $\overline{LOAD}$ = 0 in the tens digit counter, $\overline{CLR}$ = ENP = ENT = CLK = 1, and the tens digit counter realizes synchronous number setting. When the tens digit counter of the minute module is 0101 and the units digit counter is 1001, the minute module advances one bit to the hour module through the logic gate circuit.

2.2.3 Hour module design

Two 74160 counters are set in the hour module to represent the units digit and tens digit of "hours", the units digit of the "hour" is in decimal counting system, and the tens digit of "hour" is in ternary counting system. When the hour module receives the feed signal from the minute module, in the hour module, its units digit counter $\overline{CLR}$ = $\overline{LOAD}$ = ENP = ENT = CLK= 1, and the units digit counter performs the addition count of 0000-1001. When the units digit counter is 1001 its output signal RCO is high, at this time the tens digit counter $\overline{CLR}$ = $\overline{LOAD}$ = ENP = ENT = CLK= 1, the tens digit counter carries out the addition count of 0000-0010. When the tens digit counter of the hour module is 0010 and the units digit counter is 0011, the logic gate circuit is used to make the pin $\overline{LOAD}$ of the tens digit counter low, at this time, $\overline{LOAD}$ = 0 in the tens digit counter, $\overline{CLR}$ = ENP = ENT = CLK= 1, and the tens digit counter realizes synchronous number setting. The circuit design of the minute module and hour module is shown in Figure 3.

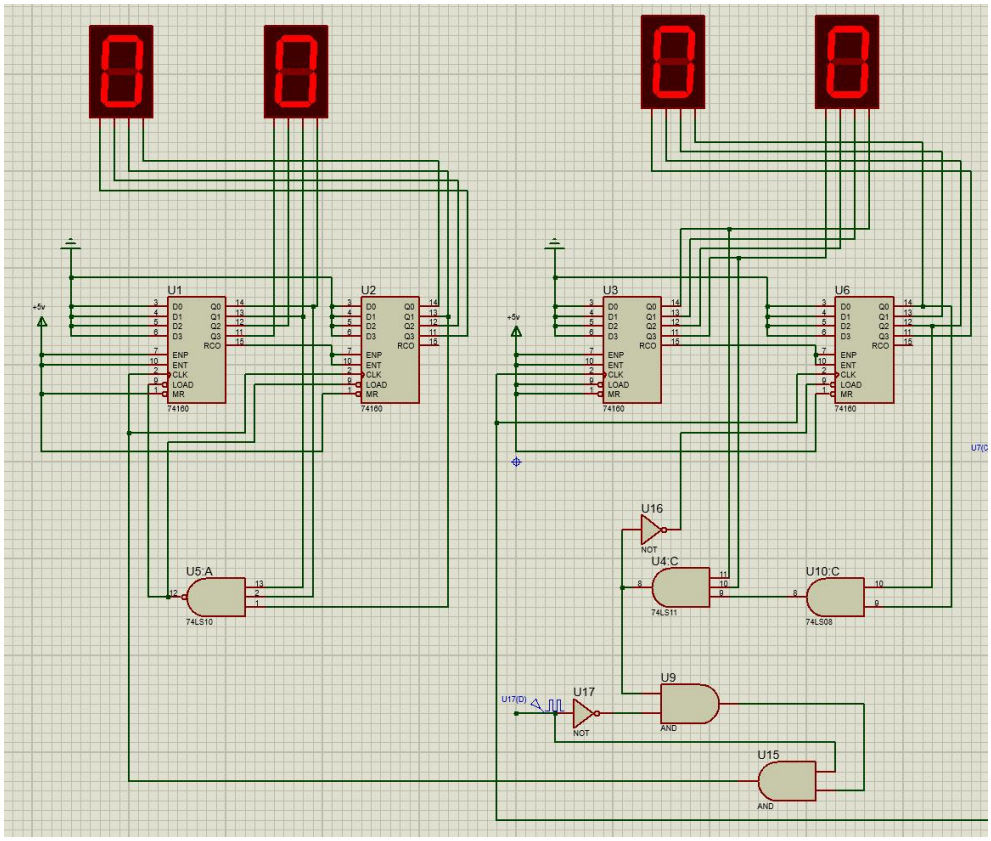

Figure 3 Minute and Hour Modules for Digital Clocks

3 DIGITAL CLOCK CIRCUIT SIMULATION

The circuit design is completed in Proteus, as shown in Figure 4. Proteus simulation software for circuit simulation, after several simulation tests, the circuit can run stably in the 00:00:00 to 23:59:59 timing range, seconds count every 60 seconds to the minutes counting bit, minutes count every 60 minutes to the hours counting bit, hours counting every 24 hours to automatically clear, the digital display is clear and no flicker. The results show that the designed clock circuit can complete the clock display function.

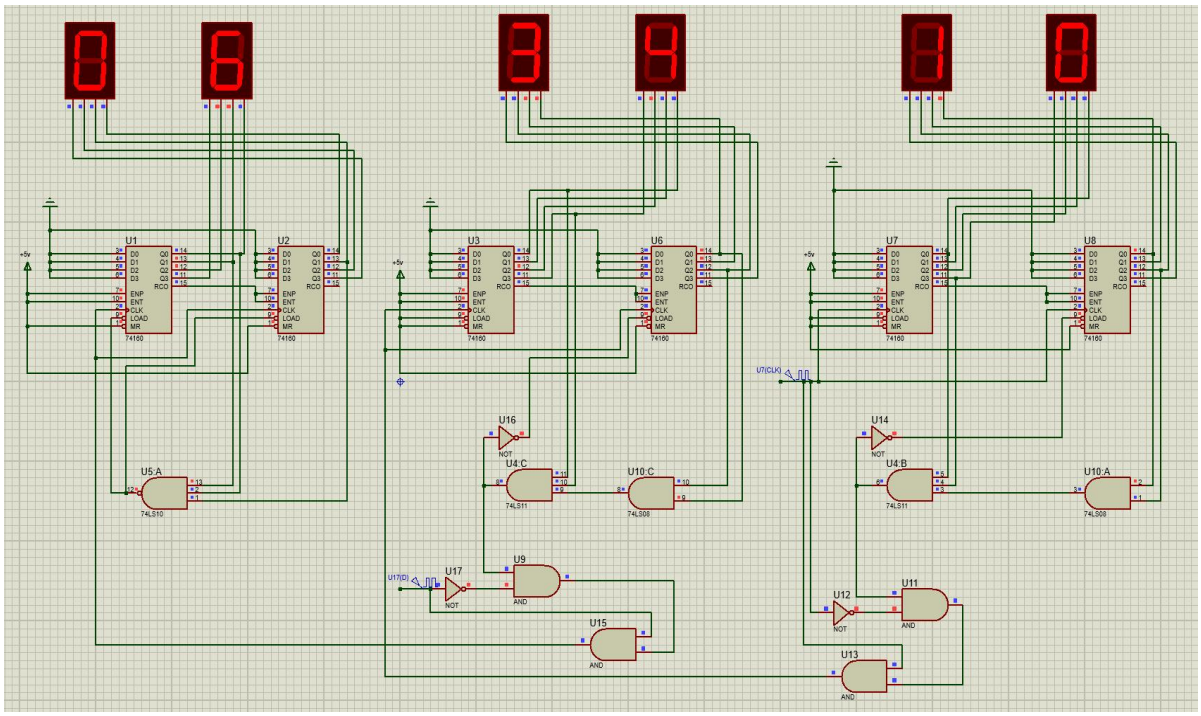

Figure 4 Digital Clock Circuit

4 CONCLUSION

In this paper, a digital clock circuit is designed and simulated using Proteus simulation software. After repeated simulations, the digital clock circuit is found to be stable and reliable, covering the range from 00:00:00 to 23:59:59. The seconds module sends a feed signal to the minutes module every 60 seconds, and the minutes module triggers a feed to the hours module every 60 minutes, while the hours module follows the 24-hour cycle rule and resets to 00:00:00 after 23:59:59, which is in line with the daily time flow pattern. The simulation results are satisfactory, which is helpful for understanding and mastering the principle of digital clock in the process of study and research. On the basis of the existing digital clock design, we deepen the innovation from the dimension that is more in line with the law of technological evolution and the actual needs of users, so as to make the classic circuit design revitalized in the application scenarios of the new era. Under the premise of maintaining the simplicity of the core counting circuit, we introduce energy-saving design to respond to the needs of low-carbon development, and develop modular adaptation solutions for multiple scenarios. The digital clock has the ability to adapt to the extension of functions in the intelligent era, so that this traditional design in the process of technology iteration continues to play a role in connecting the traditional electronic design and modern engineering applications bridge.

COMPETING INTERESTS

The authors have no relevant financial or non-financial interests to disclose.

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